In the specification:

Title

The amended title of the invention, submitted by applicant on August 13, 2007, is still not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. *Please amend the title as follows:*

"A Method and Apparatus for Multiprocessor Embedded Debugging Support Via Breakpoint Bit Fields and Debug Register Field Manipulation"

Abstract

The abstract of the disclosure stands objected to because it does not sufficiently describe the disclosure and, therefore, does not assist readers in deciding whether there is a need for consulting the full patent text for details. *Please amend the abstract as follows:*

"In one embodiment, an apparatus and method for multiprocessor debugging support via breakpoint bit fields and debug register field manipulation is disclosed. In one embodiment, the apparatus comprises a memory, a plurality of processors coupled to the memory, and a controller coupled to the memory and the plurality of processors. In addition, the controller executes a debug process that: attaches at least one breakpoint bit field directly to one or more instructions of the plurality of processor, the breakpoint bit field to enable a user of the apparatus to set a breakpoint based on an address of the particular instruction without having to perform an address comparison; manipulates at least three debug register bit fields of at least one processor control status register, the at least three register bit fields comprise a run field, a single step field, and a debug enable field; and accesses an internal status of one or more of the plurality of processors by

utilizing at least one of a Load to Instruction RAM instruction (LDTI) and a Load from Instruction RAM (LDFI) instruction. Other embodiments are also described. ~~A device having at least one processor is connected to a controller and a memory. The controller executes a debug process. The debug process adds a breakpoint bit field to each instruction. Also, a system includes image signal processors (ISPs). Each ISP includes processor elements (PEs). The ISPs also include a debug instruction register connected to a first mux element. An instruction memory is connected to an instruction register. A decoder is also connected to the instruction register. An execution unit is connected to the decoder. A debug executive unit is connected to the instruction memory, and a second mux element is connected to the execution unit and local registers. The decoder decodes a breakpoint bit field of each instruction.~~"

Detailed Description

Please amend paragraph [0047] as follows:

[0047] The above debug process embodiments can also be stored on a device or machine-readable medium and be read by a machine to perform instructions. The machine-readable medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read-only memory (ROM); random-access memory (RAM); magnetic disk storage media; optical storage media; ~~and~~ flash memory devices;~~[[.]]~~ and biological, electrical, and mechanical systems. The device or machine-readable medium may include a micro-electromechanical system (MEMS), nanotechnology devices, organic, holographic, solid-state memory device and/or a

rotating magnetic or optical disk. The device or machine-readable medium may be distributed when partitions of instructions have been separated into different machines, such as across an interconnection of computers.